sub a1

1. A method of forming a strained semiconductor layer, comprising the steps of:

providing a first wafer with a surface comprising of a first semiconductor layer of a first natural lattice constant;

forming a second semiconductor layer with a second natural lattice constant on the first semiconductor layer;

providing a second wafer with a surface with or without an insulator layer;

bonding said second semiconductor layer on said surface of said second wafer, resulting in a third wafer comprised of said second wafer, said second semiconductor layer, and said first wafer; and

performing a cleaving procedure so that said second semiconductor is separated from said first semiconductor layer and said second wafer.

2. The method of claim 1, wherein said second wafer is a single crystalline silicon substrate.

3. The method of claim 1, wherein said second wafer is a single crystalline silicon substrate with an overlying insulator layer formed on it.

4. The method of claim 3, wherein said insulator layer is a silicon dioxide layer.

5. The method of claim 3, wherein said insulator layer is a silicon nitride layer.

6. The method of claim 1, wherein said first semiconductor layer has a lattice constant greater than that of overlying said second semiconductor layer.

7. The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising silicon and germanium.

8. The method of claim 1, wherein said first semiconductor layer is an alloy semiconductor layer comprising of silicon and germanium, epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

9. The method of claim 1, wherein said second semiconductor alloy layer is a silicon layer under tensile strain.

10. The method of claim 1, wherein said second semiconductor layer is a silicon layer, epitaxially grown to a thickness between about 20 to 1000 Angstroms.

11. A method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) device on an insulator layer, featuring a silicon channel region, comprising the steps of:

providing a first wafer with a surface comprising of a first semiconductor material of a first natural lattice constant;

forming a second semiconductor layer with a second natural lattice constant on the first semiconductor material so that the said second semiconductor layer is strained;

providing a second wafer comprising of a substrate with an overlying insulator layer;

bonding said second semiconductor layer on said second wafer, with or without an insulator in between, resulting in a third wafer comprised of said second wafer, said second semiconductor layer, and said first wafer;

performing a cleaving procedure so that said second semiconductor layer is separated from said first semiconductor material, resulting in a fourth wafer comprised of said second semiconductor layer and said second wafer; and

forming a MOSFET device on the said fourth wafer, comprising of a gate structure and of source and drain regions located adjacent to said gate structure.

12. The method of claim 11, wherein said second wafer is a silicon wafer with an insulator formed on it.

13. The method of claim 12, wherein said insulator layer is a silicon dioxide layer.

14. The method of claim 12, wherein said insulator layer is a silicon nitride layer.

15. The method of claim 11, wherein said first semiconductor material is an alloy semiconductor layer comprising of silicon and germanium in a relaxed state.

16. The method of claim 15, wherein said alloy semiconductor layer is obtained by epitaxial growth procedures.

17. The method of claim 15, wherein said alloy semiconductor layer is epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

18. The method of claim 11, wherein said second semiconductor layer is a silicon layer.

19. The method of claim 18, wherein said silicon layer is epitaxially grown to a thickness between about 20 to 1000 Angstroms.

20. An ultra thin body metal oxide semiconductor field effect transistor (MOSFET), device on an insulator layer, featuring a strained semiconductor channel layer, comprising:

a strained semiconductor channel layer on an underlying insulator layer;

a gate insulator layer on said strained semiconductor channel layer;

a gate structure on said gate insulator layer; and

source/drain structures adjacent to said gate structure.

21. The ultra thin body MOSFET device of claim 20, wherein said strained semiconductor channel layer is thinner than 500 Angstroms.

22. The ultra thin body MOSFET device of claim 20, wherein said strained semiconductor channel layer is formed by the method of claim 1.

23. The ultra thin body MOSFET device of claim 20, wherein said gate insulator layer is comprised of silicon dioxide layer.

24. The ultra thin body MOSFET device of claim 20, wherein said strained semiconductor channel layer is comprised of silicon.

25. The ultra thin body MOSFET device of claim 24, wherein said silicon is under tensile stress.

26. The ultra thin body MOSFET device of claim 20, wherein said gate structure is comprised of polysilicon.

27. The ultra thin MOSFET device of claim 20, wherein said source/drain structures are comprised of raised source and drain structures.